REMARKS

Claims 1-9, 12, and 14 and 15 were presented for examination. In the Advisory Action dated July 11, 2006, Examiner maintained the rejections of claims 1-9, 12, 14 and 15 Office Action of April 27, 2006. In a decision of the Board of Patent Appeals and Interferences dated January 17, 2008, the board upheld the rejections. The claims, as amended, are presented above. Accordingly, claims 1-8 remain pending in the application.

Reconsideration is respectfully requested in view of the amendments to the claims and the following remarks. Reconsideration is respectfully requested in view of the amendments to the claims and the following remarks.

I. The § 103 Rejections

Claims 1-9 and 12-19 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,829,751 ("Shen").

Applicant respectfully traverses the rejections.

A. Shen Fails To Disclose Media Access Controller to Provide Communication with the Network server over a Network, Including Downloading Information for a Debugging Session,

For ease of examination, claim 1 is reproduced below. Claim 1 is directed towards an application specific integrated circuit (ASIC). The ASIC comprises:

a standard cell including a plurality of logic functions;

at least one bus coupled to at least a portion of the logic functions;

a plurality of internal signals from the plurality of logic functions; and

a field programmable gate array (FPGA) coupled to the at least one bus and the plurality of internal signals, the FPGA including a debug client function that observes and manipulates the at least one bus and the plurality of internal signals, the debug client function being in communication with a network server and including

media access controller to provide communication with the network server over a network, including downloading information for a debugging session,

comparator logic operable to compare selected ones of the plurality of internal signals coupled to the FPGA with a trigger pattern downloaded from the network server; and

storage logic operable to store a state of the selected ones of the plurality of internal signals that match the trigger pattern for later retrieval by the network server.

Shen discloses a system for designing an integrated circuit (IC) (see Abstract). More specifically, Shen discloses implementing an FPGA core that may be used to perform on-chip diagnostics that enable debugging functions, such as bus monitoring, probing, single step running, triggering, and capturing (col. 2, ll. 39-45).

However, Shen fails to teach or suggest the claims as recited in claim 1. Foremost, Shen does not disclose the network server of claim 1. The debugger workstation of Shen is directly connected with the chip using an I/O pin and a bus (3:22-30 and 5:20). On the other hand, the media access controller of claim 1 provides integrated support for a remotely located network server. One of ordinary skill in the art would understand the media access controller to support, for example, an Internet protocol stack. Advantageously, the ASIC can support debugging systems developed by different companies, and the debugging system can be developed in parallel with the ASIC (as discussed in the Specification on pp. 8-9). Shen, in disclosing a traditional local debugger, is silent with regards to the necessary components for a remotely located server. As a result, Shen also fails to disclose downloading information. Thus, Shen fails to disclose the network server and the media access control, in cooperation

with the other elements of claim 1.

Therefore, Applicants respectfully submit that clam 1, and all related claims, are patentable over Shen.

CONCLUSION

Applicant's attorney believes this application is in condition for allowance. Should any unresolved issues remain, Examiner is invited to call Applicant's attorney at the telephone number indicated below.

Respectfully submitted,

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